Go Beyond Mainframe Capping to Reduce MLC

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Modernizing how we understand what RMF/SMF means for performance and efficiency

Processor Cache Efficiency Concepts, Samples, and Demo

How to identify MLC reduction opportunities
Commonly Held Assumptions

1. After 30+ years, the SMF reporting process is mature and is as good as it gets
   Reality – Ripe for modernization - greatest potential in data is unrealized

2. SMF is for forensics and trending, no value for real-time
   Reality – it can provide valuable “sooner than real-time” visibility

3. Processors should run at 100% to maximize cost efficiency
   Reality – the rules have changed, and this means sites are wasting MLC
How to Modernize the Data Interpretation

With applied artificial intelligence techniques that utilize embedded, z/OS specific expert knowledge:

– Derive new, meaningful metrics out of the raw RMF/SMF data
– Normalize the data to properly correlate related metrics
– Incorporate knowledge of:
  • Internal component capacity limits (e.g., port throughput)
  • z/OS best practices for configuration and performance mgmt
  • Workload balance and redundancy loss identification
  • Relationship and interaction of logical and physical resources
Results of Modernizing RMF/SMF Interpretation

• New Insights...far more powerful than:
  – Nicer graphs or visualizations, or statistical pattern recognition (ITOA)

• Intelligence to dramatically improve Human Decision Making:
  – Where are problems or inefficiencies occurring or about to happen?
  – Good or Bad? Rate metrics in the context of the infrastructure
  – What metrics are related? View charts to see side by side
  – What do you want to see next? Drill down to determine root cause
Availability Intelligence

Outsmart IT Service Disruptions, Eliminate Infrastructure Inefficiency

**Prevent**
\- Avoid Imminent Disruptions
  See IT infrastructure issues before they disrupt service

**Resolve**
\- Accelerate Root Cause Discovery
  Quickly identify the true source of problems to restore service levels faster

**Optimize**
\- Safely Reduce Cost
  Save money without compromising service levels or availability

**Elevate**
\- Amplify IT Team Impact
  See what is important without guessing or wasting time

Performance, Availability

Efficiency, Cost
Optimize MLC – A Case Study

MIPS vs. Transactions

- Peak Hour Online MIPS
- Peak Day Trans (M)

[Graph showing MIPS and Transactions over time]
Initial Impact of z13

- z13 processor cycle speed is 10% slower than zEC12s
- But z13 rated capacity is 10% higher than zEC12s
- Realized processor capacity is more dependent than ever on effective utilization of processor cache
Optimize MLC – A Case Study

Impact of Cache Effectiveness on z13 Capacity:

Transaction growth, but MIPS reduced by more than 20%

10% RNI reduction = about 5% MIPS reduction
Poll Question #1 – MLC Reduction Focus
Processor Cache Concepts & Metrics
Key Metrics – Cycles Per Instruction (CPI)

• Number of processor cycles spent per completed instruction

• Processor cycles are spent either
  – Productively – executing instructions
  – Unproductively – waiting to stage data (L1 cache miss)
Cycles Per Instruction

“Estimated Instruction Complexity CPI” – function of workload

“Estimated Finite CPI” – sourcing from cache/memory
Key Metrics – Relative Nest Intensity (RNI)

• How deep into the shared cache and memory hierarchy ("nest") the processor must to go retrieve data not present in L1 cache

• Access time increases significantly for each level of cache (increasing processor wait time)

• $2.6 \times (0.4 \times L3P + 1.6 \times L4LP + 3.5 \times L4RP + 7.5 \times MEMP) / 100$

• Reducing RNI improves processor efficiency
CPI with Components of RNI

Reducing RNI improves CPI & processor efficiency
HiperDispatch

• Interfaces with PR/SM & z/OS Dispatchers to align work to logical processors (LPs) & align LPs to physical CPs

• Repeatedly dispatching the same work to the same or nearby CP is vital to optimizing processor cache hits
Vertical CP Configuration

• Based on LPAR weights PR/SM assigns logical CPs
  – Vertical High (VH) – 1-1 relationship with physical CP
  – Vertical Medium (VM) – has at least 50% share of a CP
  – Vertical Low (VL) – less than 50% share of a CP
• Work running on VHs has high probability of cache hits
• Work running on VMs & VLs is subject to running on various CPs and contending with other LPARs
Cache Data Lifetime

for all Processor Hardware Counters by Processor Complex serial

Estimated Lifetime in L1 cache (msec)

Estimated Lifetime in L2 cache (msec)

Estimated Lifetime in L3 cache (msec)

Estimated Lifetime in L4 cache (msec)
RNI Impact of Executing More Work on VHs

- 3 VHs
- 2 VMs
- 5 VHs
RNI by Logical CP

CPs 6 & 8 VMs

CPs 6 & 8 VHs
% CP Time Dispatched on VHs by CEC
Dispatched MIPS by CEC by Polarity
Dispatched MIPS by LPAR by Polarity
More Work Executing on Vertical High CPs

Reduced RNI

Fewer MIPS Consumed

MLC Reduction
Ways to Increase Work Executing on VH CPs

• Adjust LPAR weights
  – Increase weights for high CPU LPARs
  – Customize weights by shift
  – Configure fewer, larger LPARs

• Increase the number of physical CPs
  – Install additional hardware capacity
  – Utilize sub-capacity hardware models
Poll Question #2 – RNI/Vertical High
Areas of Potential Opportunity

Leveraging the visibility provided by IntelliMagic Vision into your data we offer a no-cost assessment to identify opportunities for potential MLC reduction based on reviewing several areas:

- Processor cache efficiency
- LPAR software configuration
- LPAR workload optimization
- Peak 4 hour rolling average optimization
- Batch workload optimization
MLC Reductions Achieved

- Sysplex aggregation
- Application tuning
- LPAR software stack
- LPAR workload mgmt
- Peak 4HRA optimization
- Batch management
- Processor cache efficiency

BAU: Transaction growth (+), MLC price (+), HW discount (-)

+59%  -33%
Product Demo into Key Metrics
# IntelliMagic Vision Systems Module – Overview

## Legacy
- CEC, LPAR, 4HRA (70)
- Real Storage, Paging (71)
- WLM (72)
- Channels (73)
- CF, XCF, FICON Dir. (74)
- Page Datasets (75)
- Virtual Storage (78)
- Address Space (30)

## Emerging
- PCIe/zEDC (74)
- LPAR Topology (99)
- Processor Cache (113)
- zIIP SMT* (70)
- Transaction* (72)
- SCM (Flash)* (74)
- SCRT/Usage* (89, 30)

* - GA 1Q 2017
MLC Assessment Offer
MLC Assessment Offer

Purpose:
- Identify unrealized MLC reduction opportunities

Process:
- Send IntelliMagic Data
- Analysis by IntelliMagic Experts
- Presentation of MLC Workshop Results

Cost: No charge for qualified sites in North America
What is Your Potential for Reducing Costs?

- MLC Assessment utilizes IntelliMagic Vision as a Service
- Quick, easy, intelligent visibility into your key metrics
- SMF processing is a good fit for SaaS
- Enables your team to access the interactive interface
Questions?

To request a no-charge MLC assessment: Intellimagic.com/MLC

Contact us with any questions or feedback:
Phone: 214-432-7920
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CMG imPACt 2017

November 6 – 9, 2017
Loews New Orleans Hotel