The Relatively New LSPR
and
The IBM z13 and z13s Performance Brief

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IBM

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Notes:
Performance is in Internal Throughput Rate (ITR) ratio based on measurements and projections using standard IBM benchmarks in a controlled environment. The actual throughput that any user will experience will vary depending upon considerations such as the amount of multiprogramming in the user's job stream, the I/O configuration, the storage configuration, and the workload processed. Therefore, no assurance can be given that an individual user will achieve throughput improvements equivalent to the performance ratios stated here.
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Topics

- What's "Relatively New" in the LSPR
  - and the theory and analysis behind it
- Performance drivers with z13
- z13 ITR Ratios
- Workload Variability
- Performance drivers with the z13s
- z13s ITR Ratios
LSPR: Performance Showcase for z Processors

- IBM System z provides capacity comparisons among processors based on a variety of measured workloads which are published in the Large System Performance Reference (LSPR)
- Old and new processors are measured in the same environment with the same workloads at high utilizations
- Over time, workloads and environment are updated to stay current with customer profiles
  - old processors measured with new workloads/environment may have different average capacity ratios compared to when they were originally measured
- LSPR presents capacity ratios among processors
- Single number metrics MIPS, MSUs, and SRM Constants
  - based on the ratios for
    - the "average" workload
    - the "median" customer LPAR configuration
LSPR RNI-based Workload Categories
Validated and now zPCR default

- Historically, LSPR workload capacity curves (primitives and mixes) had application names or been identified by a "software" captured characteristic
  - for example, CICS, IMS, OLTP-T, CB-L, LoI0-mix, TI-mix, etc
- However, capacity performance is more closely associated with how a workload is using and interacting with a processor "hardware" design
- With the availability of CPU MF (SMF 113) data starting with z10, the ability to gain insight into the interaction of workload and hardware exists.
- The LPSR for z196 introduced three new workload categories which replaced all prior primitives and mixes.
  - LOW, AVERAGE, HIGH Relative Nest Intensity
  - originally treated as a workload "hint" in zPCR
- Migrations to z196 and zEC12 have validated this approach
  - detailed study of 16 customers and 75 LPARs for each of the migration scenarios of z10 to z196 and z196 to zEC12
- RNI-based methodology for workload matching is now the default in zPCR
Fundamental Components of Workload Capacity Performance
Part 1

- Instruction Path Length for a transaction or job
  - Application dependent, of course
  - Can also be sensitive to Nway (due to MP effects such as locking, work queue searches, etc)
  - But generally doesn't change much on moves between processors of similar capacity and/or Nway

- Instruction Complexity (Micro processor design)
  - Many design alternatives
    - Cycle time (GHz), instruction architecture, pipeline, superscalar, Out-Of-Order, branch prediction and more
  - Workload effect
    - May be different with each processor design
    - But once established for a workload on a processor, does not change very much
Fundamental Components of Workload Capacity Performance
Part 2

- Memory Hierarchy or "nest"
  - Many design alternatives
    - cache (levels, size, private, shared, latency, MESI protocol), controller, data buses
  - Workload effect
    - Quite variable
    - Sensitive to many factors: locality of reference, dispatch rate, IO rate, competition with other applications and/or LPARs, and more

- Relative Nest Intensity
  - Activity beyond the private cache(s) is the most sensitive area
    - due to larger latencies involved
  - Reflects activity distribution and latency to chip-level caches, book-level caches and memory
  - Level 1 cache miss percentage also important
  - Data for calculation available from CPU MF (SMF 113) starting with z10
z196 versus z10 hardware comparison

- **z10 EC**
  - CPU
    - 4.4 GHz
  - Caches
    - L1 private 64k i, 128k d
    - L1.5 private 3 MB
    - L2 shared 48 MB / book
    - book interconnect: star

- **z196**
  - CPU
    - 5.2 GHz
    - Out-Of-Order execution
  - Caches
    - L1 private 64k i, 128k d
    - L2 private 1.5 MB
    - L3 shared 24 MB / chip
    - L4 shared 192 MB / book
    - book interconnect: star
The Most Influential Factor
Underlying Workload Capacity Curves is
Relative Nest Intensity (RNI)

- Many factors influence a workload's capacity curve
- However, what they are actually affecting is the workload's RNI
- It is the net effect of the interaction of all these factors that determines the capacity curve
- The chart below indicates the trend of the effect of each factor but is not absolute
  - for example, some batch will have high RNI while some transactional workloads will have low
  - for example, some low IO rate workloads will have high RNI, while some high IO rates will have low

<table>
<thead>
<tr>
<th>Low</th>
<th>High</th>
</tr>
</thead>
<tbody>
<tr>
<td>Batch</td>
<td>Transactional</td>
</tr>
<tr>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>Single</td>
<td>Many</td>
</tr>
<tr>
<td>Intensive</td>
<td>Light</td>
</tr>
<tr>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>High locality</td>
<td>Diverse</td>
</tr>
<tr>
<td>Simple</td>
<td>Complex</td>
</tr>
<tr>
<td>Extensive</td>
<td>Limited</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>Application Type</td>
<td></td>
</tr>
<tr>
<td>IO Rate</td>
<td></td>
</tr>
<tr>
<td>Application Mix</td>
<td></td>
</tr>
<tr>
<td>CPU Usage</td>
<td></td>
</tr>
<tr>
<td>Dispatch Rate</td>
<td></td>
</tr>
<tr>
<td>Data Reference Pattern</td>
<td></td>
</tr>
<tr>
<td>LPAR Configuration</td>
<td></td>
</tr>
<tr>
<td>Software Configuration Tuning</td>
<td></td>
</tr>
</tbody>
</table>
LSPR Workload Categories

- Categories developed to match the profile of data gathered on customer systems
  - over 100 data points (LPARs) used in the profiling
- Various combinations of prior workload primitives are measured on which the new workload categories are based
  - Applications include CICS, DB2, IMS, OSAM, VSAM, WebSphere, COBOL, utilities

- **LOW** (relative nest intensity)
  - Workload curve representing light use of the memory hierarchy
  - Similar to past high Nway scaling workload primitives

- **AVERAGE** (relative nest intensity)
  - Workload curve expected to represent the majority of customer workloads
  - Similar to the past LoI0-mix curve

- **HIGH** (relative nest intensity)
  - Workload curve representing heavy use of the memory hierarchy
  - Similar to the past DI-mix curve

- zPCR extends these published categories
  - Low-Avg
    - 50% LOW and 50% AVERAGE
  - Avg-High
    - 50% AVERAGE and 50% HIGH
CPU MF

- What is CPU MF?
  - A z10 GA2 and later facility that provides memory hierarchy COUNTERS
  - Also capable of time-in-Csect type SAMPLES
  - Data gathering controlled through z/OS HIS (HW Instrumentation Services)
    - Collected on an LPAR basis
    - Written to SMF 113 records
    - Minimal overhead

- How can the COUNTERS be used today?
  - To supplement current performance data from SMF, RMF, DB2, CICS, etc.
  - To help understand why performance may have changed

- How can the COUNTERS be used for future processor planning?
  - They provide the basis for the LSPR workload categories
  - zPCR can automatically processes CPU MF data to provide a workload match based on RNI

- Reference John Burg's CPU MF presentation at SHARE
  - March 3, 11:15-12:15
z196 versus z10 hardware comparison

- **z10 EC**
  - CPU
    - 4.4 GHz
  - Caches
    - L1 private 64k i, 128k d
    - L1.5 private 3 MB
    - L2 shared 48 MB / book
    - book interconnect: star

- **z196**
  - CPU
    - 5.2 GHz
    - Out-Of-Order execution
  - Caches
    - L1 private 64k i, 128k d
    - L2 private 1.5 MB
    - L3 shared 24 MB / chip
    - L4 shared 192 MB / book
    - book interconnect: star
Volunteer Customers Total CPI vs RNI

Low    | Average | High

CPU MF
z10 Customer Workload Characterization Summary
## RNI-based LSPR Workload Decision Table

<table>
<thead>
<tr>
<th>L1MP</th>
<th>RNI</th>
<th>LSPR Workload Match</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt;3</td>
<td>&gt;= 0.75</td>
<td>AVERAGE</td>
</tr>
<tr>
<td></td>
<td>&lt; 0.75</td>
<td>LOW</td>
</tr>
<tr>
<td>3 to 6</td>
<td>&gt;1.0</td>
<td>HIGH</td>
</tr>
<tr>
<td></td>
<td>0.6 to 1.0</td>
<td>AVERAGE</td>
</tr>
<tr>
<td></td>
<td>&lt; 0.6</td>
<td>LOW</td>
</tr>
<tr>
<td>&gt;6</td>
<td>&gt;=0.75</td>
<td>HIGH</td>
</tr>
<tr>
<td></td>
<td>&lt; 0.75</td>
<td>AVERAGE</td>
</tr>
</tbody>
</table>

Notes: Applies to all processors z10 and later
Table may change based on feedback
Performance Drivers with z13

- **Hardware**
  - memory subsystem
    - continued focus on keeping data "closer" to the processor unit
      - larger L1, L2, L3, L4 caches
      - improved IPC (Instructions Per Cycle) aka reduced CPI (Cycles Per Instruction)
    - 3x configurable memory
  - processor
    - 2x instruction pipe width, re-optimized pipe depth for power/performance
      - improved IPC aka reduced CPI
    - SMT for zIIPs and IFLs
      - includes metering for capacity, utilization and adjusted chargeback (zIIPs)
    - SIMD unit for analytics
    - up to 8 processor units per chip
    - up to 141 configurable processor units
    - 4 different uni speeds

- **HiperDispatch**
  - exploits new chip configuration
  - required for SMT on zIIPs

- **PR/SM**
  - 85 customer partitions (up from 60)
  - memory affinity
    - keep LPAR's CPs and memory local to drawer as much as possible
**z13 versus zEC12 hardware comparison**

**zEC12**
- CPU
  - 5.5 GHz
  - Enhanced Out-Of-Order
- Caches
  - L1 private 64k i, 96k d
  - L2 private 1 MB i + 1 MB d
  - L3 shared 48 MB / chip
  - L4 shared 384 MB / book

**z13**
- CPU
  - 5.0 GHz
  - Major pipeline enhancements
- Caches
  - L1 private 96k i, 128k d
  - L2 private 2 MB i + 2 MB d
  - L3 shared 64 MB / chip
  - L4 shared 480 MB / node
    - plus 224 MB NIC
z13 Capacity Performance Highlights

- Full speed capacity models ... capacity ratio to zEC12
  - average 1.10x at equal Nway
  - average 1.40x max capacity (141w z13 versus 101w zEC12)

- Subcapacity models
  - Uniprocessor capacity ratio to full speed z13
    - 0.15x (target 250 MIPS)
    - 0.44x
    - 0.63x
  - up to 30 CPs (general purpose processors) for each subcap model

- SMT capacity option
  - IFL's and zIIPs can optionally choose to run 2 HW threads per processor engine or "core"
    - opt-in or opt-out at the LPAR level
    - added HW threads appear as additional logical processors to z/VM and z/OS
  - may see wide range in capacity improvement per core over single thread: +10% to +40%

- Variability amongst workloads
  - workloads moving to z13 can expect to see more variability than last migration
    - performance driven by improved IPC in core and nest
      - workloads will not react the same to the improvements in these areas
      - micro benchmarks are particularly susceptible to this effect
SMT Overview

- SMT allows for the enablement of a second hardware thread per processor engine or "core"
  - Appears as another logical processor to z/VM and z/OS
  - LPARs may opt-in or opt-out to SMT on IFLs or zIIPs

- Capacity gain per core will vary
  - Dependent on the overlap and interference between the two threads
    - overlap
      - many core resources are replicated so each thread can make progress
      - while one thread waits for a cache miss, the other thread can continue to run
    - interference
      - some serialization points within the core
      - threads share the same caches, thus cache misses can increase
  - Benchmarks observe +10% to +40% capacity increase versus single HW thread per core
    - no clear predictor of where a workload will fall

- With SMT, individual tasks (SW threads) run slower but dispatcher delays reduce
  - For example, a 1.3x capacity gain is spread over 2 HW threads which means each thread runs at 1.3/2 = .65x a single thread or about the speed of a z196 core
  - But with twice as many HW threads (logical processors) to dispatch to, dispatching delays (CPU queuing) can be reduced

- Metering available through RMF and z/VM Performance Reports
  - Thread density, utilization, capacity factors
What's new in the LSPR for z13 and z13s

- Workload updates
  - upleveled software - z/OS 2.1, subsystems, compilers
  - minor tweaks to three hardware-characteristic-based workload categories
    - based on CPU MF data from customers' z196 to zEC12 migrations

- HiperDispatch continues to be turned on for all measurements
  - important even on smaller Nway processors starting with z196 and above due to sensitivity to
    L3 chip-level cache

- LSPR will publish only single HW thread capacity in the multi-image table
  - multi-image (MI) table
    - median LPAR configuration for each model based on customer profile
      - including effect of average number of ICFs and IFLs
    - most representative for vast majority of customers
    - basis for single-number metrics MIPS, MSUs, SRM constants

- zPCR allows any configuration to be modelled
  - customized LPAR configurations and workloads (as always)
  - SMT capacity effect will be included via a user controlled "dial"
    - set dial to reflect the estimated capacity increase of 2 threads over 1 thread
    - pre-install guidance in setting dial to be provided based on internal testing and eventual
      field experience (Defaults to 20% for IFLs, 25% for zIIPs)
    - post-install guidance in setting dial from metering data available in RMF and z/VM
      Performance Reports
Median LPAR Configuration Profiles for the Multi-image Table

- Total number of z/OS images
  - 5 images at low-end models to 9 images at high-end
- Number of major images (>20% weight each)
  - 2 images across full range of models
- Size of images
  - low- to mid-range models have at least one image close to Nway of model
  - high-end models generally have largest image well below Nway of model
  - these models tend to be used for consolidation
- Logical to physical CP ratio
  - low-end near 5-1
  - most of the range 2-1
  - high-end near 1.3-1
- Book configuration
  - 1 "extra" book beyond what is needed to contain CPs
- ICFs/IFLs
  - 3 ICFs/IFLs
Using the LSPR z/OS V2R1 Tables

- For the most accurate capacity sizing...
  - use zPCR customized LPAR configuration planning function
    - should always be used for final configuration planning for any upgrade
- LSPR tables may be used for high level capacity comparisons
  - Multi-image table represents average LPAR configuration and is the basis for all single-number metrics
- Tables at the LSPR website and those in zPCR will have slight differences
  - Precision
    - LSPR rounded to two digits to right of decimal point
    - zPCR carries maximum significant digits internally (displayed result is rounded to show 5 significant digits for the largest processor)
  - Reference (base) processor
    - LSPR fixed at 2094-701
    - zPCR chosen by you (the user)
**LSPR website z/OS V2R1 Tables**

**z13 versus zEC12**

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### Multi Image Table

<table>
<thead>
<tr>
<th>z/OS V2R1 AVERAGE</th>
<th>z/OS V2R1 AVERAGE</th>
<th>z/OS V2R1 AVERAGE</th>
<th>z/OS V2R1 AVERAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>zEC12 ITR</td>
<td>z13 ITR</td>
<td>z13:zEC12 ratio</td>
<td>z13 PCI</td>
</tr>
<tr>
<td>701</td>
<td>2.70</td>
<td>3.03</td>
<td>1.12</td>
</tr>
<tr>
<td>708</td>
<td>17.98</td>
<td>19.99</td>
<td>1.11</td>
</tr>
<tr>
<td>716</td>
<td>31.98</td>
<td>35.13</td>
<td>1.10</td>
</tr>
<tr>
<td>732</td>
<td>55.85</td>
<td>61.55</td>
<td>1.10</td>
</tr>
<tr>
<td>764</td>
<td>98.70</td>
<td>108.44</td>
<td>1.10</td>
</tr>
<tr>
<td>7A1</td>
<td>140.10</td>
<td>154.99</td>
<td>1.11</td>
</tr>
<tr>
<td>z13 7E1 vs zEC12 7A1</td>
<td>140.10</td>
<td>199.28</td>
<td>1.42</td>
</tr>
</tbody>
</table>

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z13 includes 3 subcapacity offerings

Subcapacity Offerings vs Full Speed

<table>
<thead>
<tr>
<th>z13</th>
<th>z/OS V2R1 MI AVG ITRR</th>
<th>Ratio to 701</th>
<th>PCI</th>
<th>Max #CPs</th>
</tr>
</thead>
<tbody>
<tr>
<td>701</td>
<td>3.03</td>
<td>1.00</td>
<td>1695</td>
<td>141</td>
</tr>
<tr>
<td>601</td>
<td>1.91</td>
<td>.63</td>
<td>1068</td>
<td>30</td>
</tr>
<tr>
<td>501</td>
<td>1.33</td>
<td>.44</td>
<td>746</td>
<td>30</td>
</tr>
<tr>
<td>401</td>
<td>.45</td>
<td>.15</td>
<td>250</td>
<td>30</td>
</tr>
</tbody>
</table>

Notes: Uni speeds range from 15% to 63% of full speed uni
Each subcapacity offering has a maximum of 30 CPs
Workload Variability with z13

- Performance variability is generally related to fast clock speed and physics
  - increasing memory hierarchy latencies relative to micro-processor speed
  - increasing sensitivity to frequency of "missing" each level of processor cache
  - workload characteristics are determining factor, not application type

- z13 performance comes from improved IPC (instructions per cycle) in both the micro-processor and the memory subsystem (clock speed is 10% slower but tasks run on average 10% or more faster)
  - magnitude of improvement in IPC will vary by workload
  - workloads moving into a z13 will likely see more variation than last migration

- Examples of workload variation for moves to new technology starting with the z9 appear on the next few slides
LSPR Single Image Capacity Ratios
10way: z10 EC versus z9 EC
Example of Workload Variability

LSPR Workload

LOW RNI | AVERAGE RNI | HIGH RNI
---|---|---
1.60 | 1.51 | 1.42

CB-L individual job capacity ratios

Capacity Ratio
LSPR Single Image Capacity Ratios
10way: z196 versus z10 EC
Example of Workload Variability

LSPR Workload

- LOW RNI: 1.32
- AVERAGE RNI: 1.38
- HIGH RNI: 1.44
LSPR Single Image Capacity Ratios
16way: zEC12 versus z196
Example of Workload Variability

LSPR Workload

- LOW RNI: 1.27
- AVERAGE RNI: 1.24
- HIGH RNI: 1.22
LSPR Single Image Capacity Ratios
16way: z13 versus zEC12
Example of Workload Variability

LSPR Workload

CB-L individual job capacity ratios

Capacity Ratio

LOW RNI  AVERAGE RNI  HIGH RNI

1.14  1.10  1.06

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Performance Drivers with z13s

- **Hardware**
  - memory subsystem
    - continued focus on keeping data "closer" to the processor unit
    - larger L1, L2, L3, L4 caches (>=2x larger)
    - improved IPC (Instructions Per Cycle)
    - 8x configurable memory (up to 4 TBs total)
  - processor
    - 2x instruction pipe width, re-optimized pipe depth for power/performance
    - improved IPC
    - SMT for zIIPs and IFLs
      - includes metering for capacity, utilization and adjusted chargeback (zIIPs)
    - SIMD unit for analytics
    - up to 7 processor units per chip
  - up to 20 configurable processor units
  - 26 different uni speeds

- **HiperDispatch**
  - exploits new chip configuration
  - required for SMT on zIIPs

- **PR/SM**
  - 40 customer partitions (up from 30)
  - memory affinity
    - keep LPAR's CPs and memory local to drawer as much as possible
    - usually z13s will stay in 1st drawer as 1st 2 TBs of memory is placed in the 1st drawer
z13s versus zBC12 hardware comparison

- **zBC12**
  - CPU
    - 4.2 GHz
    - Enhanced Out-Of-Order
  - Caches
    - L1 private 64k i, 96k d
    - L2 private 1 MB i + 1 MB d
    - L3 shared 24 MB / chip
    - L4 shared 192 MB / book

- **z13s**
  - CPU
    - 4.3 GHz
    - Major pipeline enhancements
  - Caches
    - L1 private 96k i, 128k d
    - L2 private 2 MB i + 2 MB d
    - L3 shared 64 MB / chip
    - L4 shared 480 MB / node
    - plus 224 MB NIC
z13s Capacity Performance Highlights

- Full speed capacity models ... capacity ratio to zBC12
  - improved Nway scaling (much larger L3 and L4)
  - 1.3x to 1.5x for equal Nway based on workload and Nway
  - >1.4x max capacity for CPs (6w z13 MR versus 6w zBC12)
  - >2x max capacity for IFLs (20w z13 MR versus 13w zBC12)

- 156 capacity settings provide wide range of capacity
  - uni speeds approximately 6% to 91% of full speed
  - A01: 80 MIPS
  - Z01: 1430 MIPS
  - Z06: 7123 MIPS

- SMT capacity option
  - IFL’s and zIIPs can optionally choose to run 2 HW threads per processor engine or "core"
  - opt-in or opt-out at the LPAR level
  - added HW threads appear as additional logical processors to z/VM and z/OS
  - may see wide range in capacity improvement per core over single thread:
    +10% to +40%
### LSPR z/OS V2R1 Tables
#### z13s versus zBC12

Examples from the Multi Image Table

<table>
<thead>
<tr>
<th></th>
<th>z/OS V2R1 AVERAGE</th>
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<th>z/OS V2R1 AVERAGE</th>
</tr>
</thead>
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<tr>
<td></td>
<td>zBC12 ITR</td>
<td>z13s ITR</td>
<td>z13s:zBC12 ratio</td>
<td>z13s PCI</td>
</tr>
<tr>
<td>Z01</td>
<td>1.90</td>
<td>2.55</td>
<td>1.34</td>
<td>1430</td>
</tr>
<tr>
<td>Z06</td>
<td>8.86</td>
<td>12.72</td>
<td>1.44</td>
<td>7123</td>
</tr>
</tbody>
</table>
z13s includes 25 subcapacity offerings

**Example Uni-processor Offerings vs Full Speed**

<table>
<thead>
<tr>
<th>z13s</th>
<th>z/OS V2R1 MI AVG</th>
<th>Ratio to Z01</th>
<th>PCI</th>
<th>Max #CPs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Z01</td>
<td>2.55</td>
<td>1.00</td>
<td>1430</td>
<td>6</td>
</tr>
<tr>
<td>A01</td>
<td>0.14</td>
<td>.06</td>
<td>80</td>
<td>6</td>
</tr>
<tr>
<td>G01</td>
<td>0.31</td>
<td>.12</td>
<td>172</td>
<td>6</td>
</tr>
<tr>
<td>T01</td>
<td>1.33</td>
<td>.52</td>
<td>746</td>
<td>6</td>
</tr>
</tbody>
</table>

Notes: Uni speeds range from 6% to 91% of full speed uni
Summary

- "Relatively New" RNI-based LSPR
  - Validated and is the default in zPCR

- z13 traditional performance
  - approximately 10% more capacity per engine than zEC12
  - max config provides approximately 40% more capacity vs zEC12

- z13 new performance opportunities
  - 3x memory
  - SMT for IFLs and zIIPs add another 10% to 40% per engine capacity
  - SIMD for analytics

- z13s
  - 26 capacity models with uni speeds ranging from 80 to 1430 MIPS
  - up to 6 general purpose processors, up to 20 total configurable processors
  - 8x memory, SMT for IFLs and zIIPs, SIMD for analytics

- Workload variability will be higher than past few generations